The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended): A semiconductor package comprising:

a die having a plurality of layers of low-K dielectric material in the die, the die having a **[[active]] top** surface including circuitry fabricated thereon, a non-active surface **not including circuitry**, and a plurality of side surfaces, each surface having associated corner and edge regions;

a wire bonding packaging substrate having a plurality of electrical contacts, the packaging substrate being positioned under the die;

a plurality of interconnects electrically connecting the die to the plurality of electrical contacts;

a molding interface material applied to at least a portion of the **[[active]] top** surface of the die, the molding interface material being configured to control at least one of tensile and shear stresses experienced by the die in the proximity of the active surface; and

a molding cap **including a molding compound** covering at least a portion of the die, packaging substrate, interconnects, and the molding interface material;

wherein the molding interface material is a discrete layer separate from the molding compound and formed between the molding cap and the die.

2. (Previously Presented): A semiconductor package as recited in claim 1, wherein the molding interface material is configured to introduce compressive stress to the die and strengthen the die against the at least one of tensile and shear stresses.

3. (Previously Presented): A semiconductor package as recited in claim 1, wherein the molding interface material is either polyimide or BCB.

4. (Previously Presented): A semiconductor package as recited in claim 1, wherein the molding interface material is on at least a portion of the plurality of side surfaces of the die.

5. (Previously Presented): A semiconductor package as recited in claim 4, wherein the molding interface material is also on a corresponding adjacent portion of the packaging substrate in order to secure the die to the packaging substrate.

6. (Currently Amended): A semiconductor package as recited in claim 1, wherein the molding interface material is applied in multiple non-contiguous regions to the **[[active]]** **top** surface of the die.

7. (Original): A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is rectangular in shape.

8. (Original): A semiconductor package as recited in claim 6, wherein at least one of the multiple non-contiguous regions is triangular in shape.

9. (Original): A semiconductor package as recited in claim 6, wherein each of the multiple non-contiguous regions has a thickness of less than 2 microns.

10. (Currently Amended): A semiconductor package as recited in claim 1, wherein the molding interface material is a contiguous region on the **[[active]]** **top** surface of the die excluding corner regions.

11. (Original): A semiconductor package as recited in claim 10, wherein the contiguous region is offset from the corner regions by about 100 to 150 microns.

12. (Currently Amended): A semiconductor package as recited in claim 10, wherein the molding interface material is a contiguous region on the **[[active]]** **top** surface of the die excluding edge regions.

13. (Original): A semiconductor package as recited in claim 12, wherein the contiguous region is offset from the edge regions by about 100 to 150 microns.

14. (Original): A semiconductor package as recited in claim 1, wherein the molding

15. (Currently Amended): A semiconductor package as recited in claim 14, wherein the molding interface material is over a substantial portion of the **[[active]]** **top** surface of the die such that a stress buffer zone is established between the **[[active]]** **top** surface of the die and the molding cap.

16. (Original): A semiconductor package as recited in claim 1, wherein the plurality of layers includes extra low-K dielectric material.

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37. (Previously Presented): A semiconductor package a recited in claim 1, wherein the molding interface material is a layer positioned between and in contact with the die and the molding cap.

38. (Previously Presented): A semiconductor package as recited in claim 1, wherein the plurality of layers of low-K dielectric material have a CTE between the range of 20 ppm and 50 ppm.

39. (Previously Presented): A semiconductor package as recited in claim 1, wherein the plurality of layers of low-K dielectric material have a dielectric constant between 2.6 and 3.5.

40. (Previously Presented): A semiconductor package as recited in claim 1, wherein the plurality of layers of low-K dielectric material have a dielectric constant between 2.2 and 2.6.